A 90 nm Communication Technology Featuring SiGe HBT Transistors, RF CMOS, Precision R-L-C RF Elements and 1 μm^2 6-T SRAM Cell

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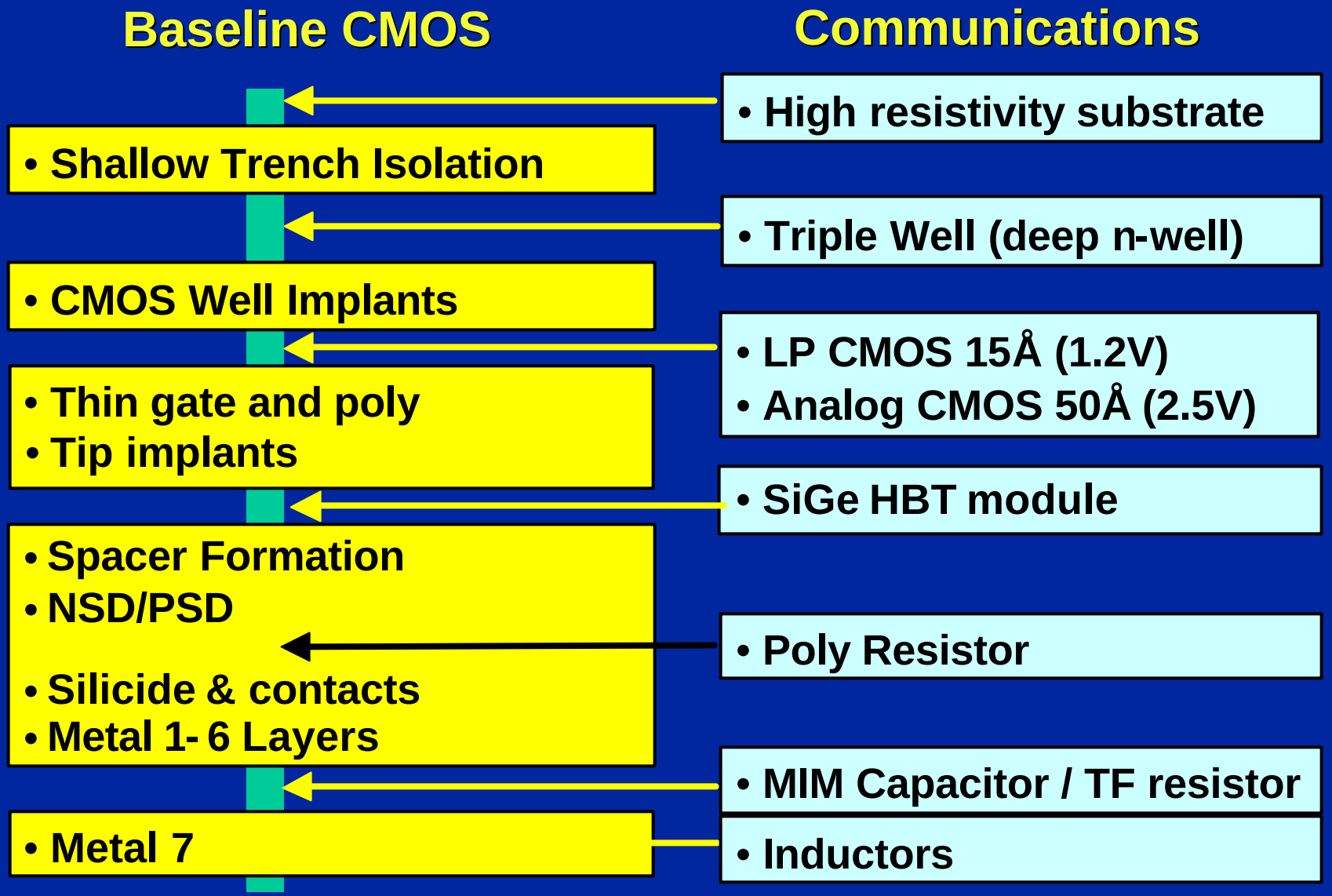
Logic Technology Development

Intel Corporation, Hillsboro, OR 97124, USA

Outline

- Technology Features
- CMOS
- SiGe:C HBT
- Isolation
- Passives
- Validation Vehicles
- Conclusions

Integration

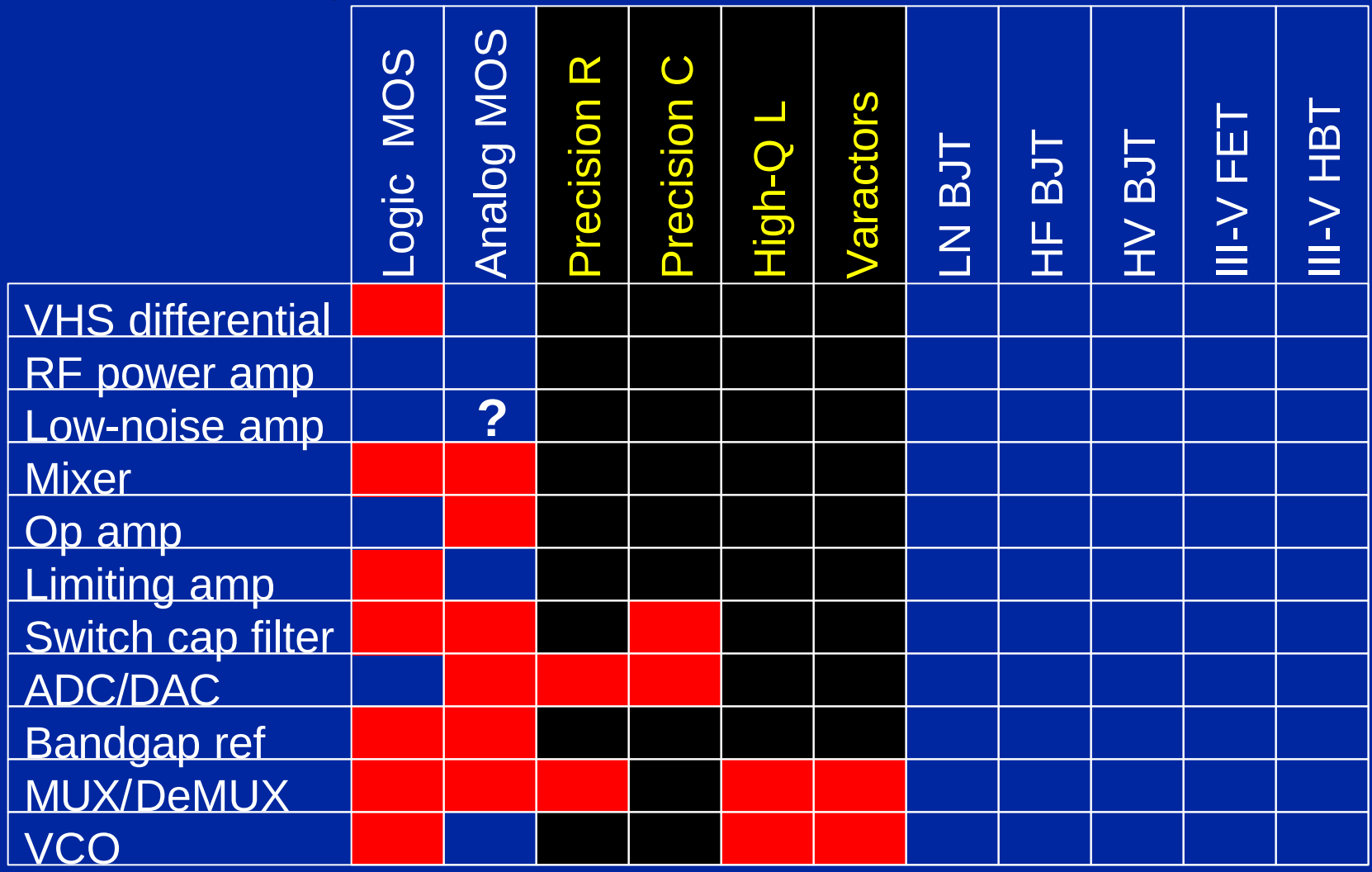


Matching Circuit Needs to Device Type

	Logic MOS	Analog MOS	Precision R	Precision C	High-Q L	Varactors	LN BJT	HF BJT	HV BJT	III-V FET	III-V HBT
VHS differential											
RF power amp											
Low-noise amp		?									
Mixer											
Op amp											
Limiting amp											
Switch cap filter											
ADC/DAC											
Bandgap ref											
MUX/DeMUX											
VCO											

Logic and analog MOS are the foundation for the majority of critical communications circuits

Matching Circuit Needs to Device Type



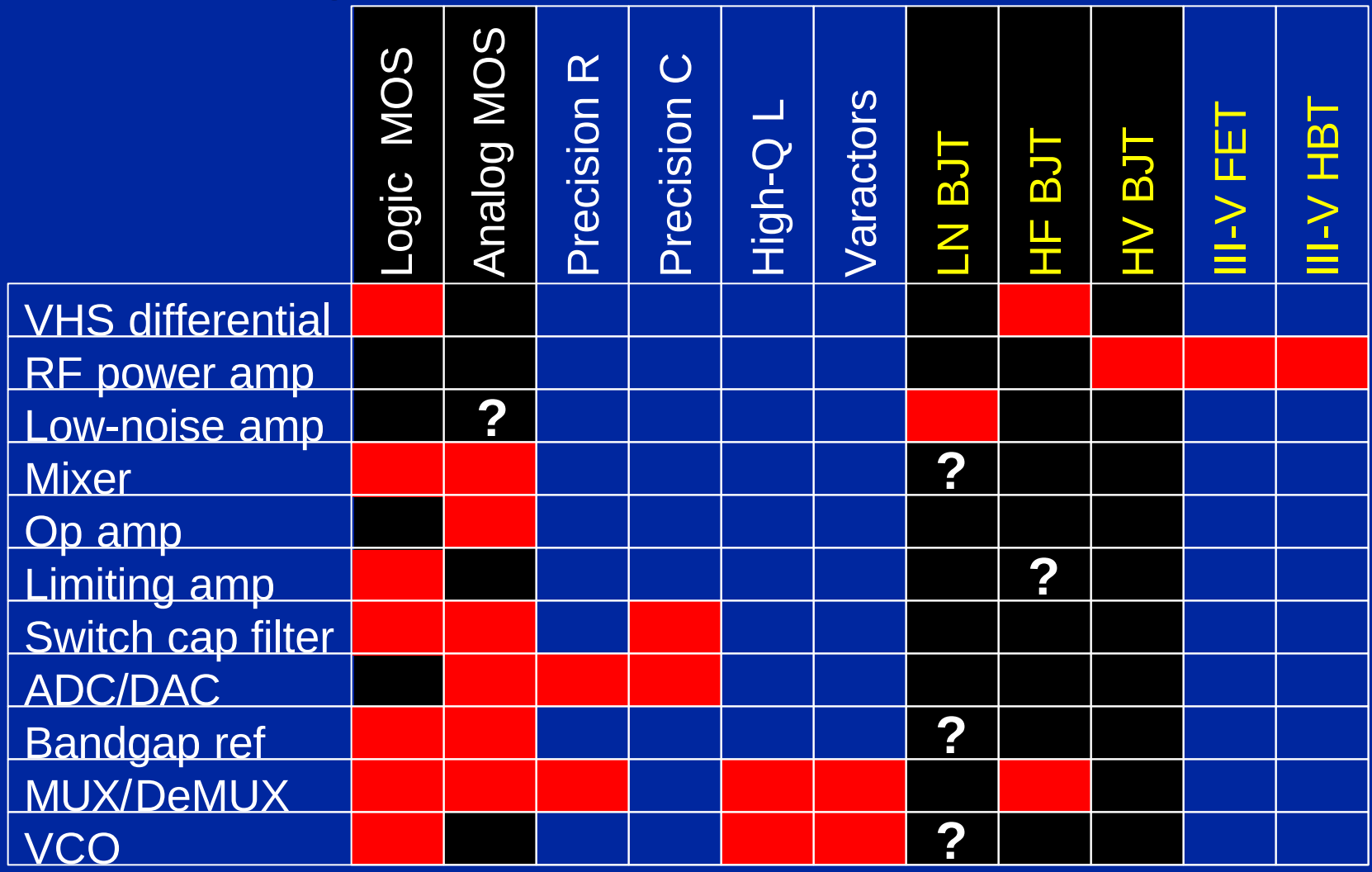
Precision single elements are key to many circuits

Matching Circuit Needs to Device Type

	Logic MOS	Analog MOS	Precision R	Precision C	High-Q L	Varactors	LN BJT	HF BJT	HV BJT	III-V FET	III-V HBT
VHS differential	■							■			
RF power amp									■	■	■
Low-noise amp		?					■				
Mixer	■	■					?				
Op amp		■									
Limiting amp	■							?			
Switch cap filter	■	■		■							
ADC/DAC		■	■	■							
Bandgap ref	■	■					?				
MUX/DeMUX	■	■	■		■	■		■			
VCO	■				■	■	?				

Most circuits have multiple implementation paths, redundancy is important in process definition

Matching Circuit Needs to Device Type

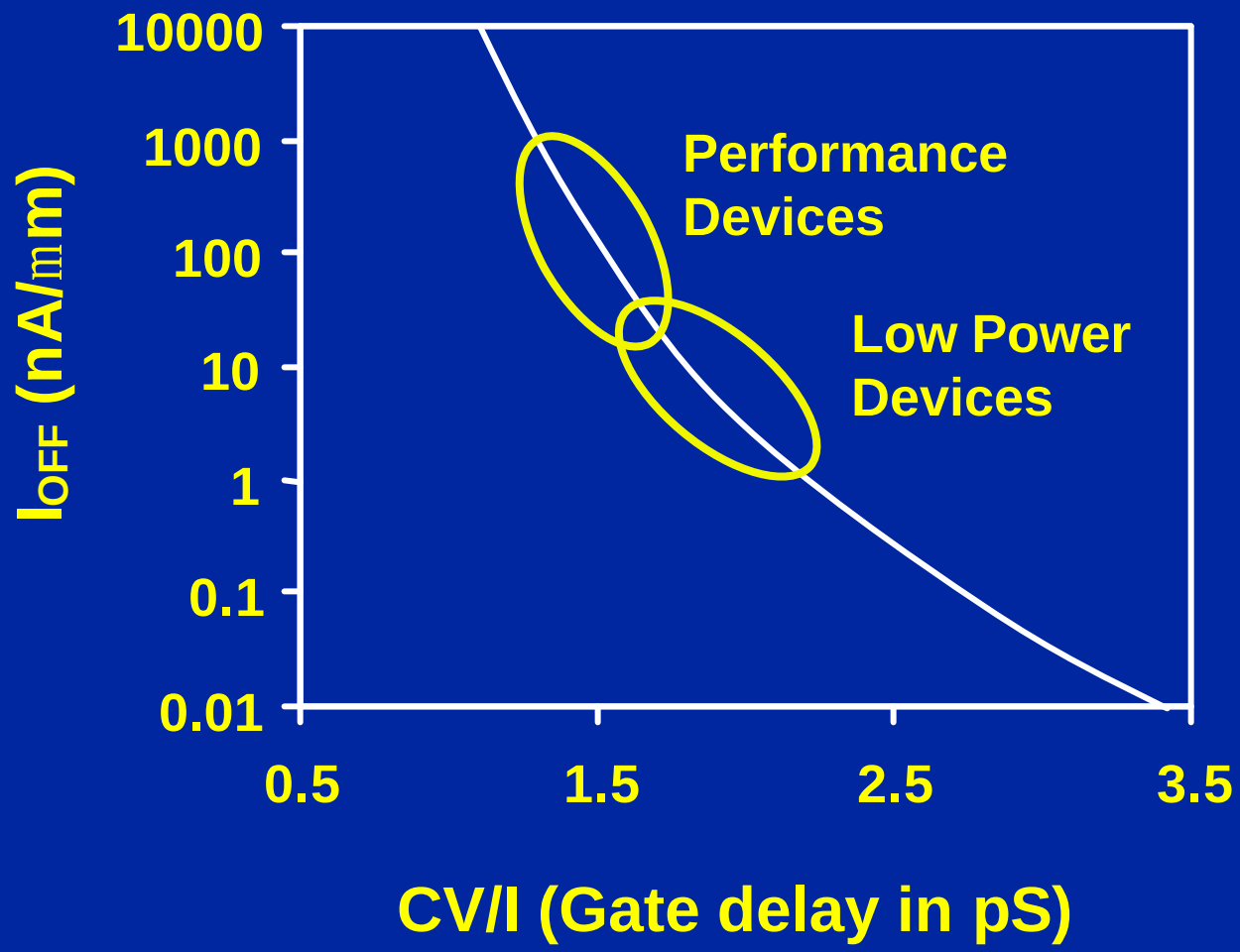


Specialized BJT devices cover gaps where MOS falls short

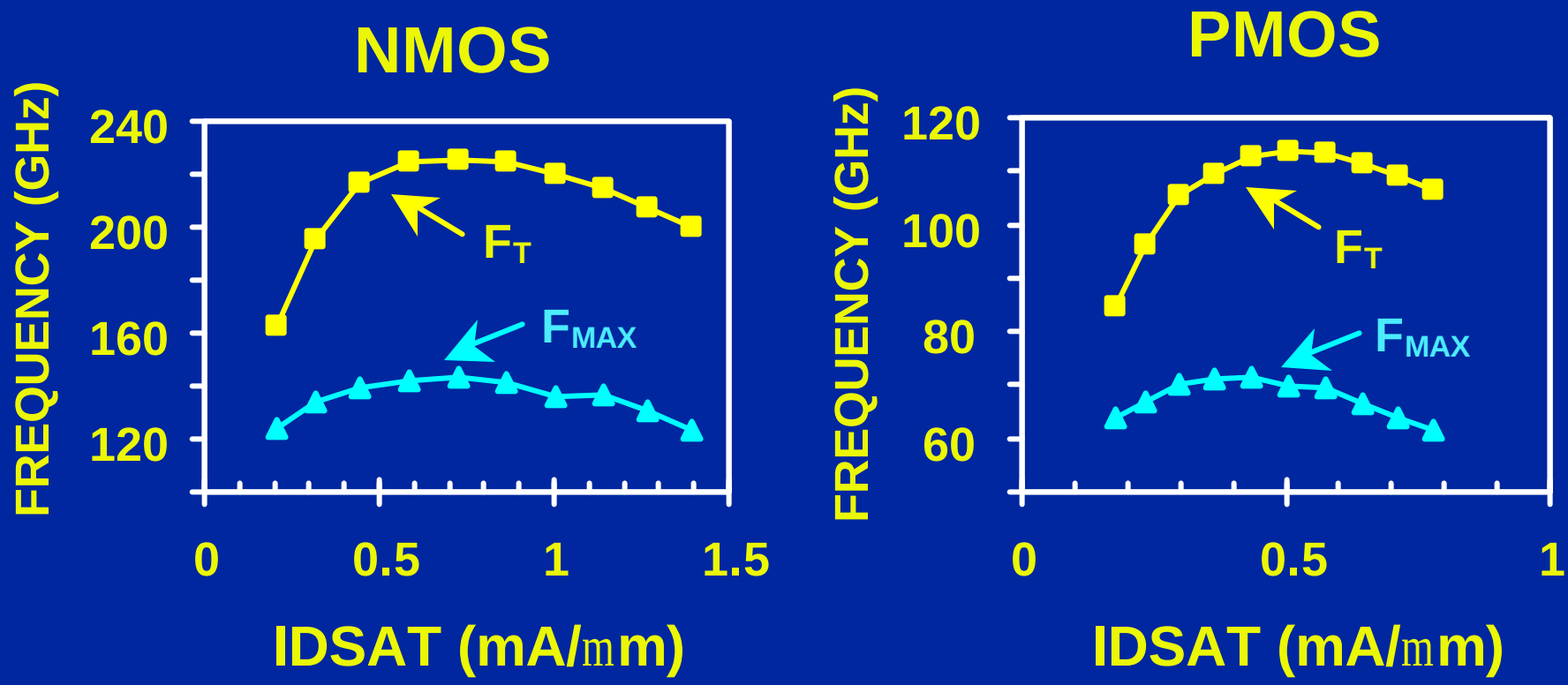
Outline

- Technology Features
- CMOS

90nm CMOS
Performance versus Low Power

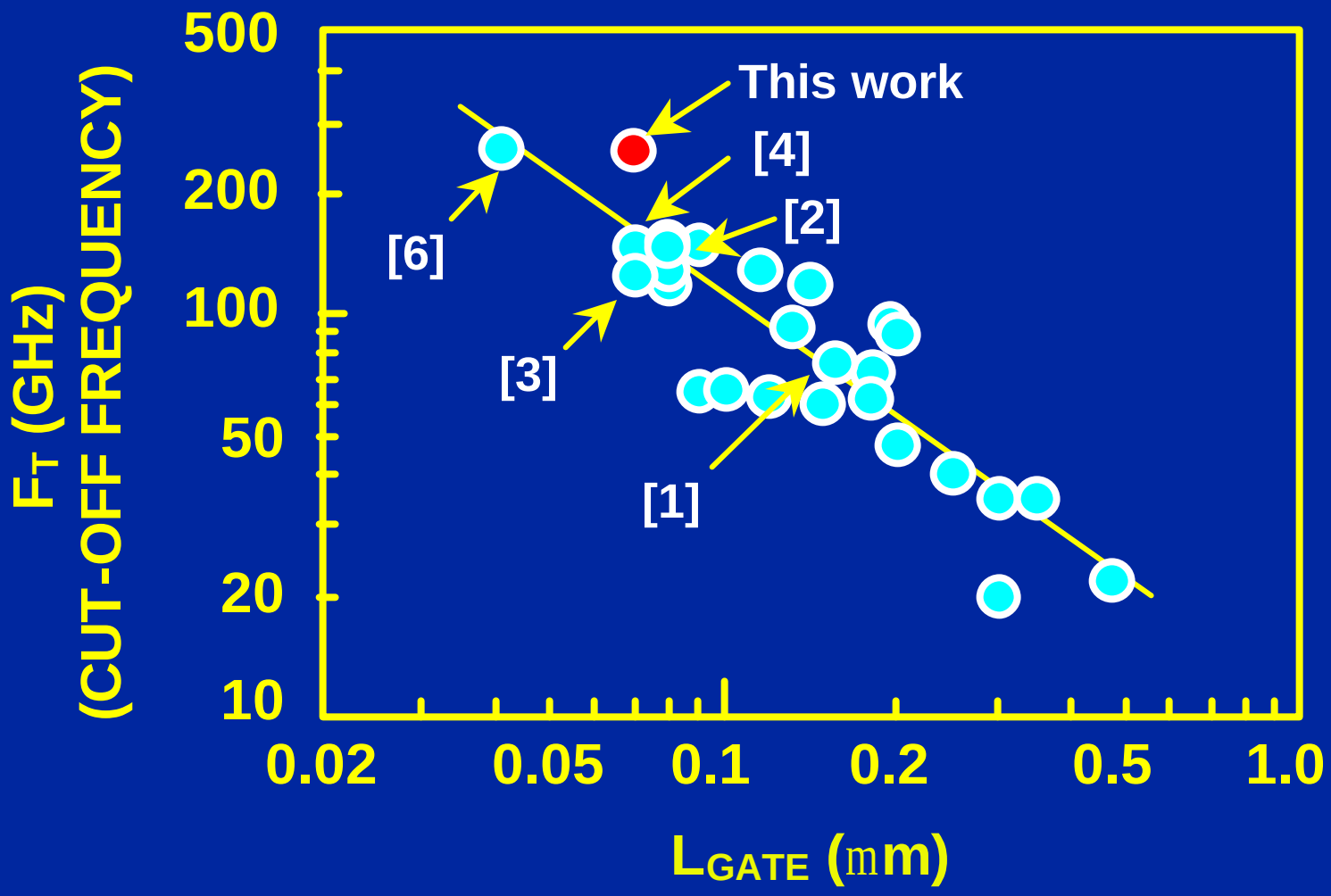


90nm Communications CMOS
RF Performance (Low Power Device)

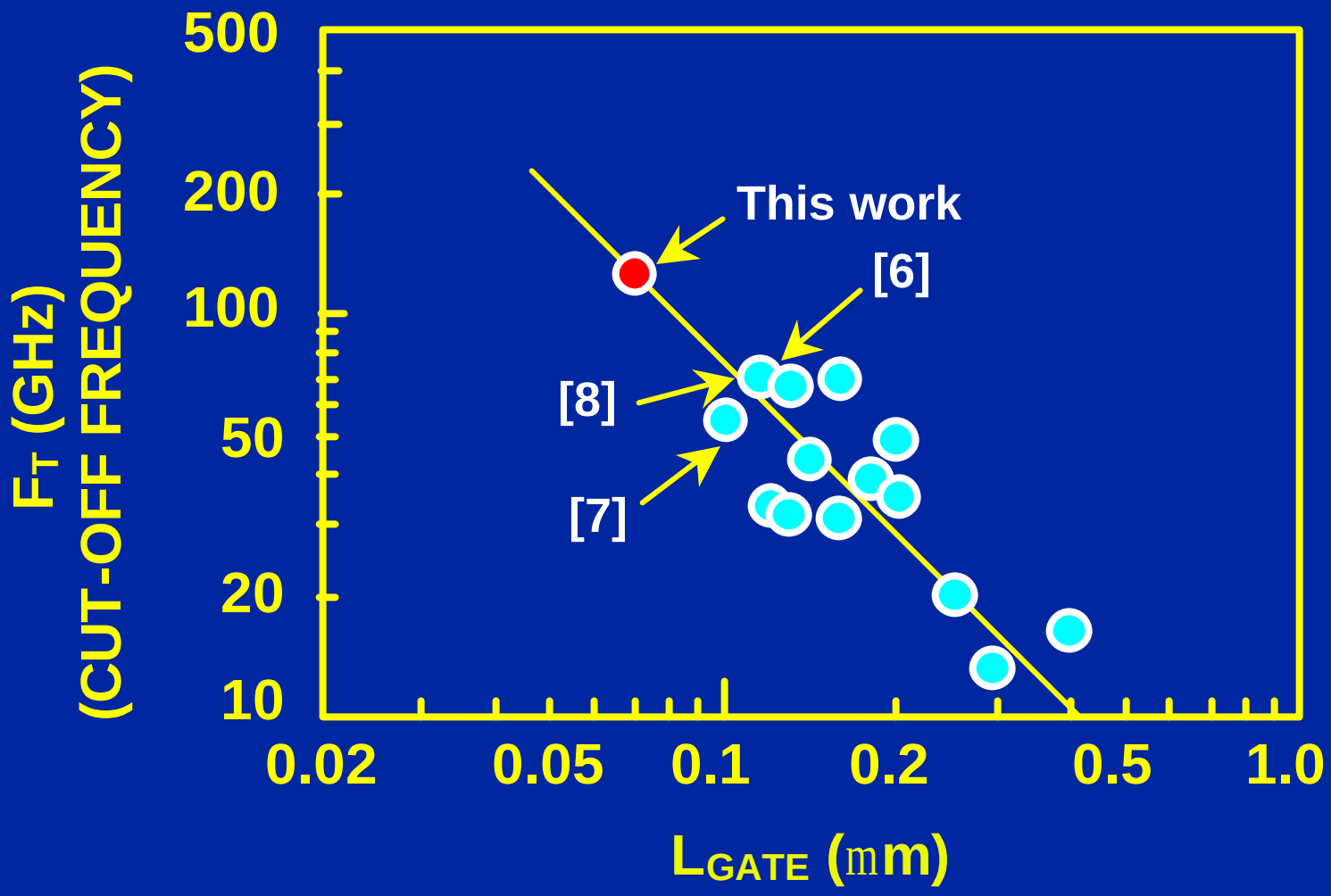


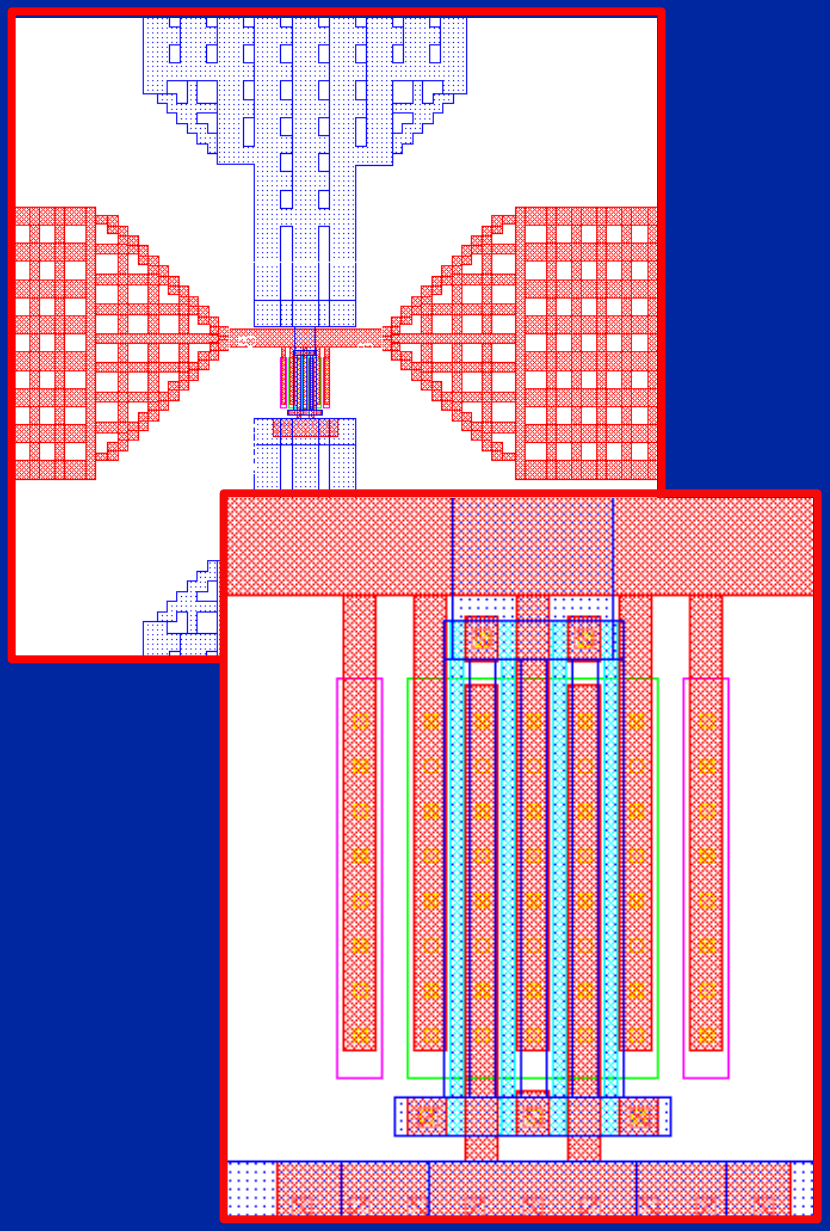
NMOS: 225/143 F_T/F_{MAX}
PMOS: 114/70 F_T/F_{MAX}
(Vg=0.7V, Vds=1.2V)

F_T: Intrinsic NMOS Performance



F_T: Intrinsic PMOS Performance



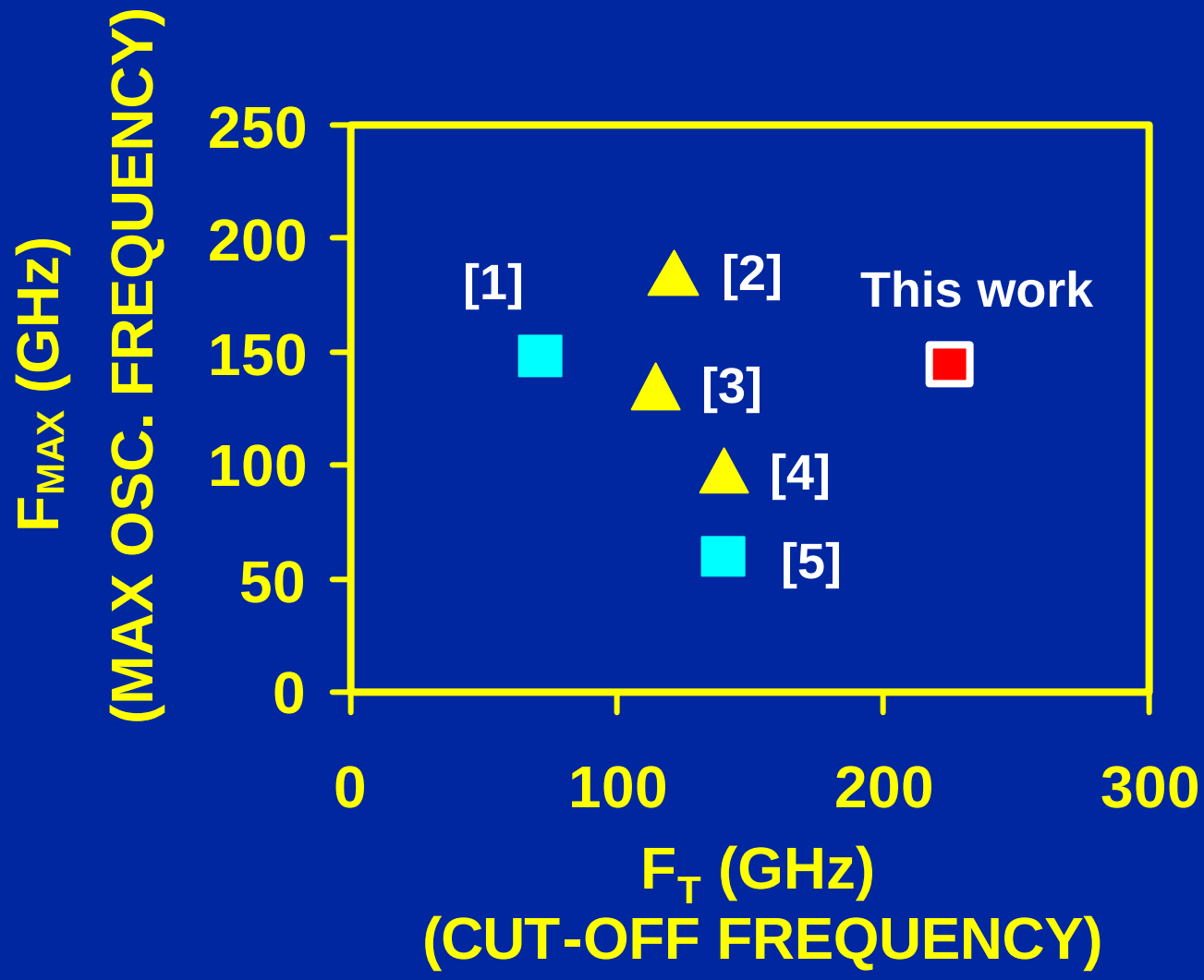


Fmax: Layout

- **Make R_G small**
  - Two-sided gates
  - Minimize field extension
  - Contacts close to devices
  - Multiple fingers
- **Minimize pad coupling**
  - HiRES substrates
  - Isolate / shield signal pads
  - Use higher-level metal
- **Minimize cap / scatter**
  - Isolate gate from drain
  - Taper source bus

Similar to: L. F. Tiemeijer, et al. "A record high 150 GHz fmax realized at 0.18 um gate length in an industrial RF-CMOS technology," IEDM 2001.

Comparison of CMOS: F_T and F_{MAX}



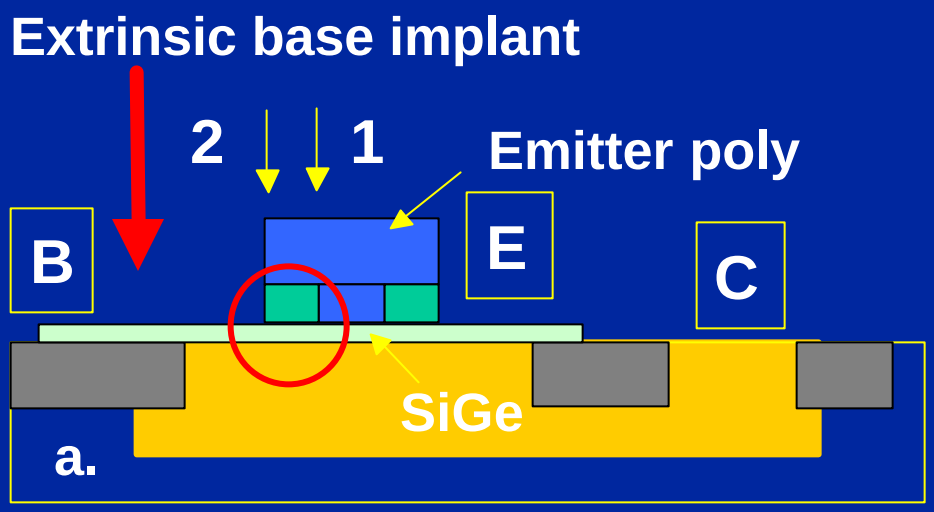
Outline

- Technology Features
- CMOS
- SiGe:C HBT

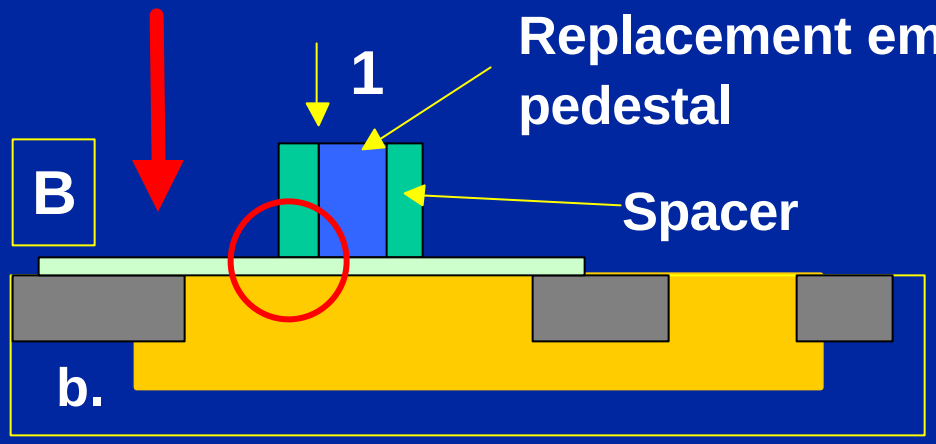
Criteria for BJT device definition

- Manufacturing simplicity
- Maximum leverage of the main 90nm microprocessor process (all tools shared, no special tools)
- Meets the needs of the circuit design community
- No impact to CMOS performance

SiGe:C HBT Architecture



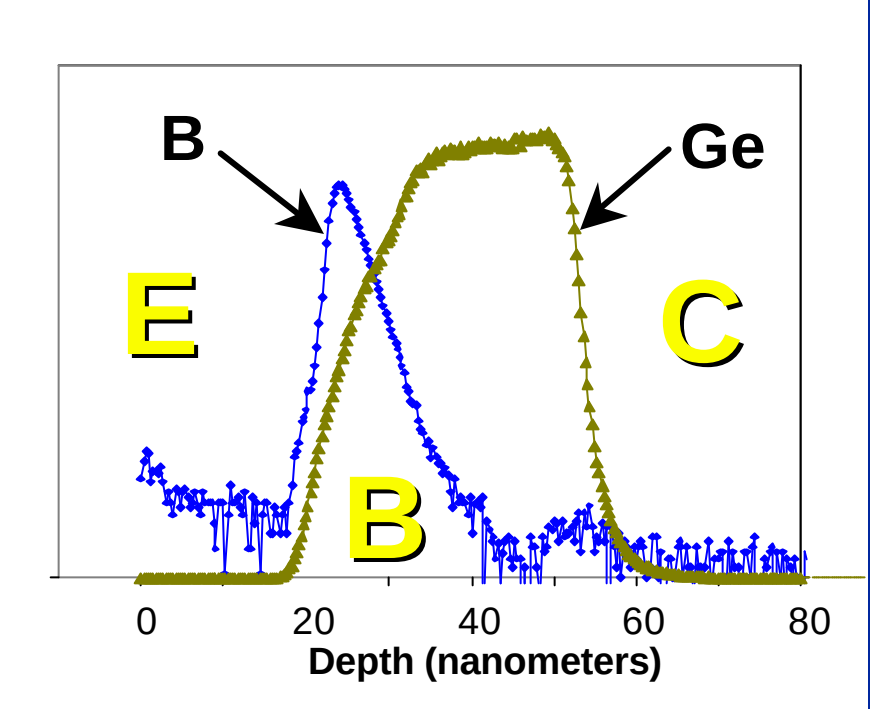
Quasi-Self-aligned



Fully Self-aligned

Quasi-self-aligned chosen as the better tradeoff between manufacturing complexity and performance

HBT: SiGe:C Epitaxy

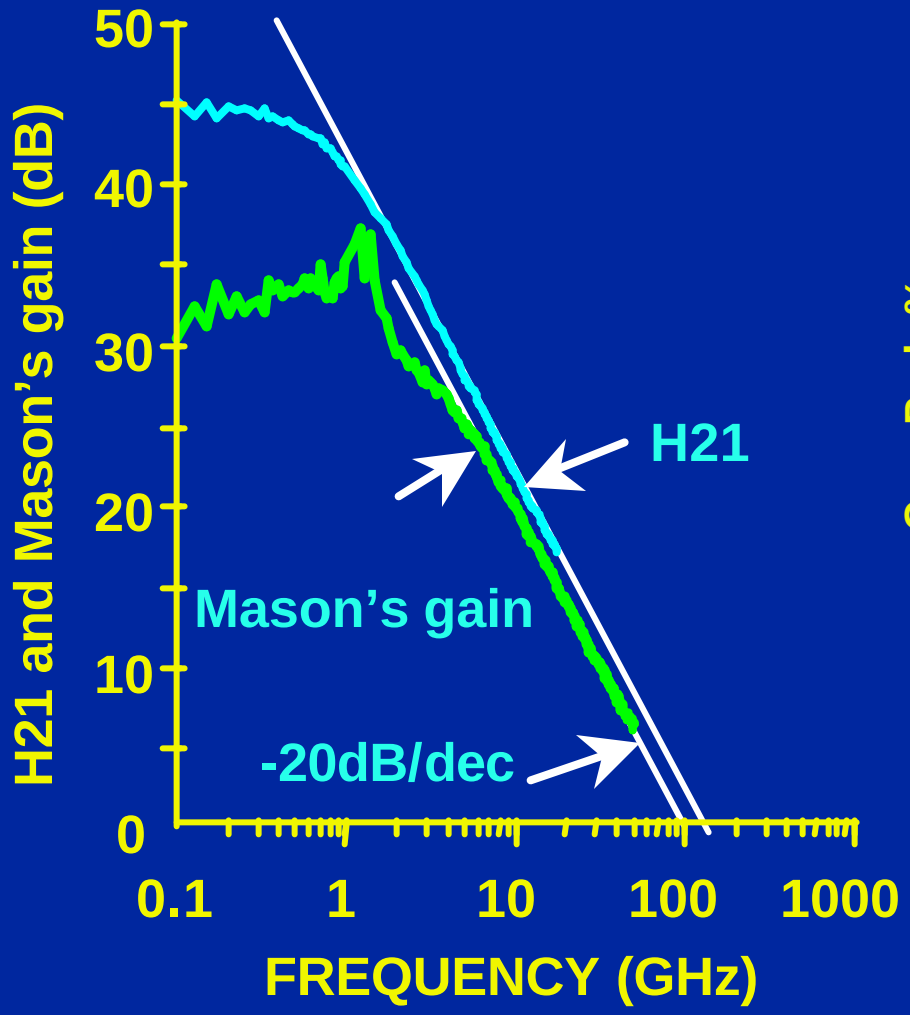


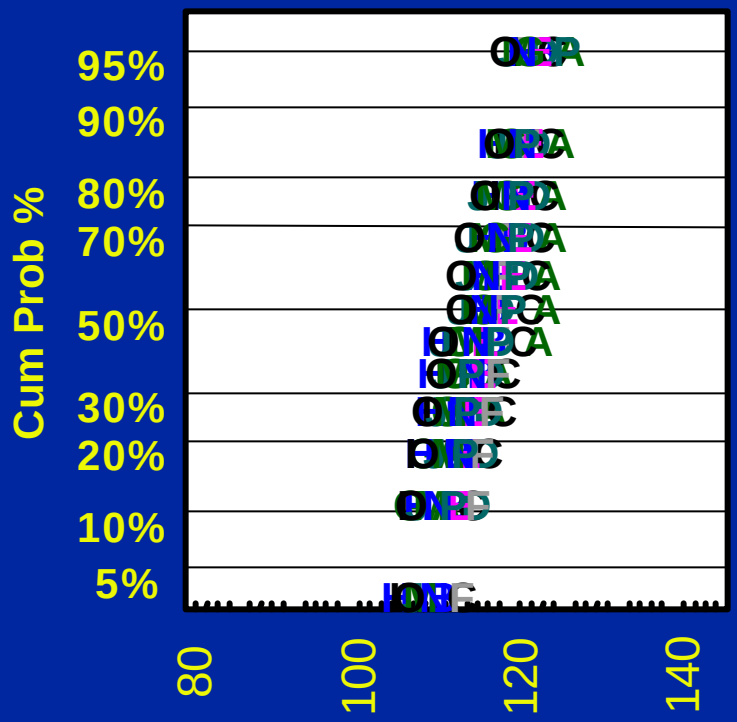
G.L. Patton, et al. "**SiGe-base heterojunction bipolar transistors: physics and design issues,"** Electron Devices Meeting, 1990.

L.D. Lanzerotti et al. "**Suppression of boron outdiffusion in SiGe HBTs by carbon incorporation,"** Electron Devices Meeting, 1996

H.J. Osten, et al. "**The effect of carbon incorporation on SiGe heterobipolar transistor performance and process margin,"** Electron Devices Meeting, 1997.

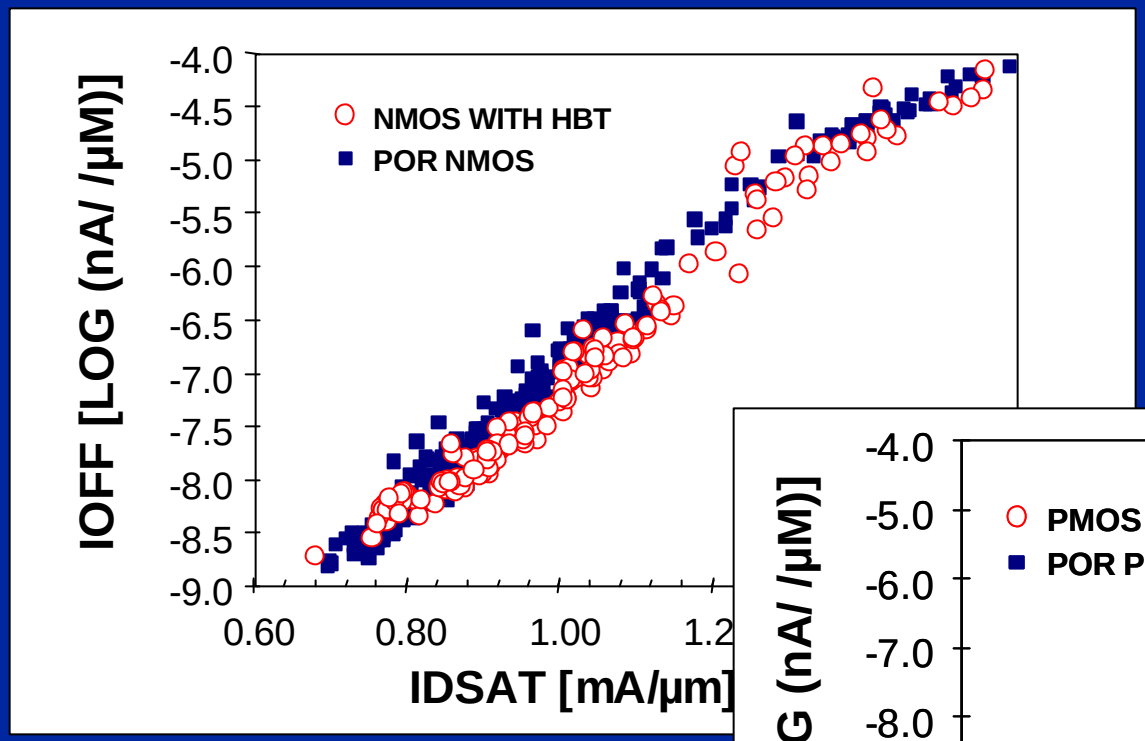
Baseline: 130/100 F_T/F_{MAX}



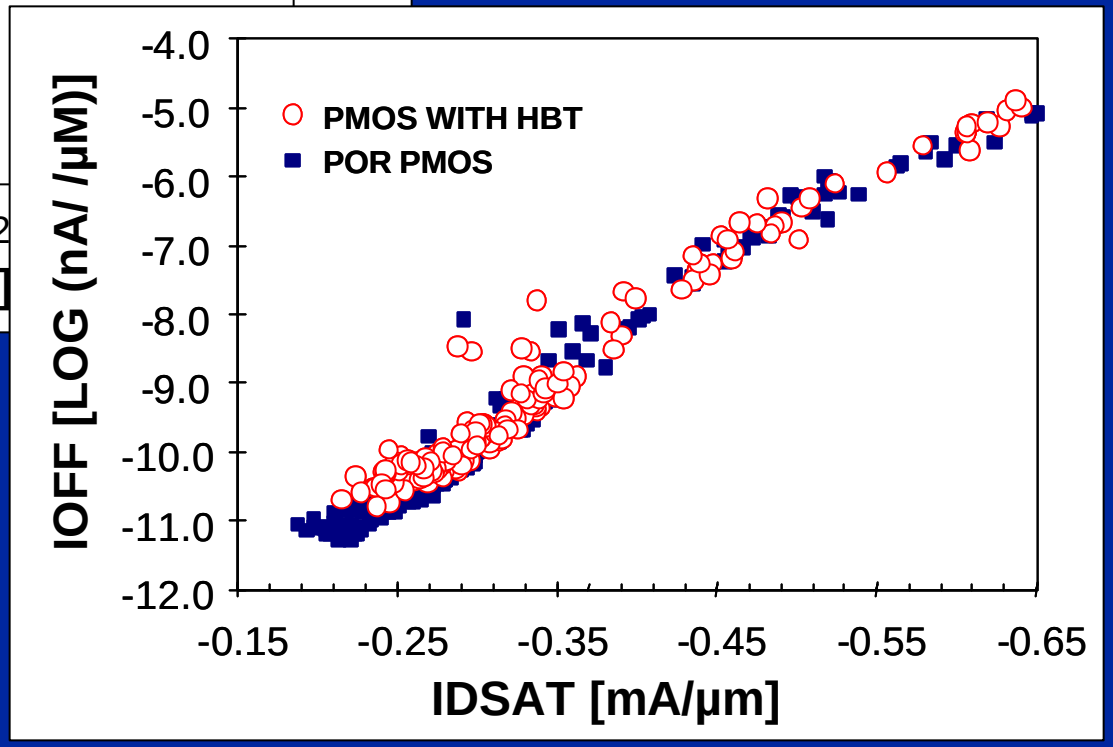


300 mm BASELINE LOT, WIW and WTW F_T VARIATION (GHz)

No CMOS Degradation

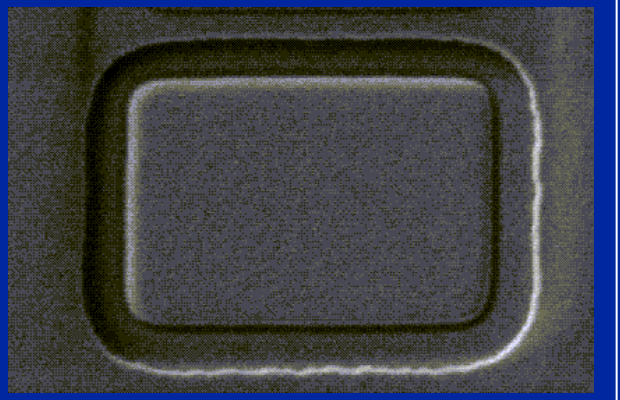


- NMOS and PMOS I_{ON} versus I_{OFF} characteristics are not degraded by HBT integration

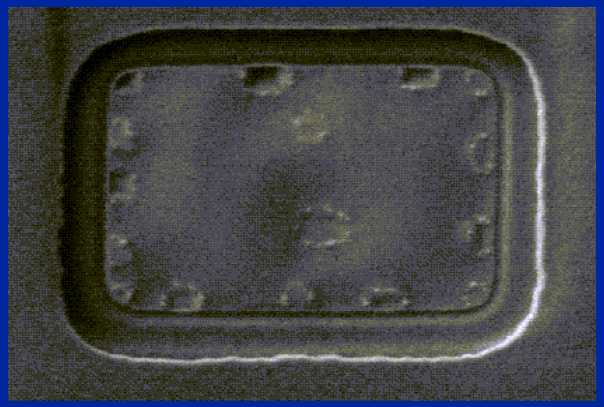


BJT Yield issues: impact of volume

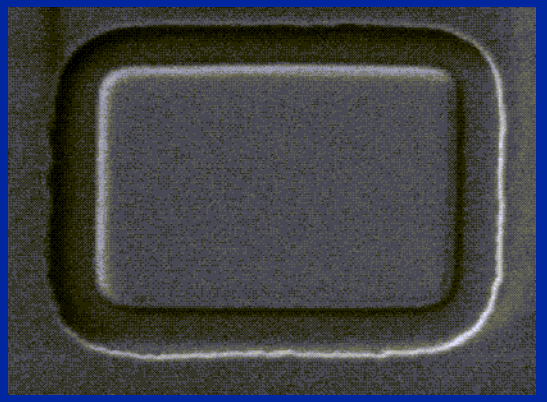
Incoming to EPI



OLD Process
Start of epi dep

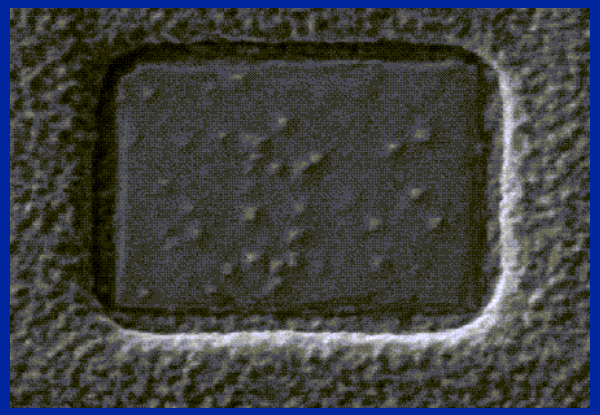


NEW Process
Start of epi dep

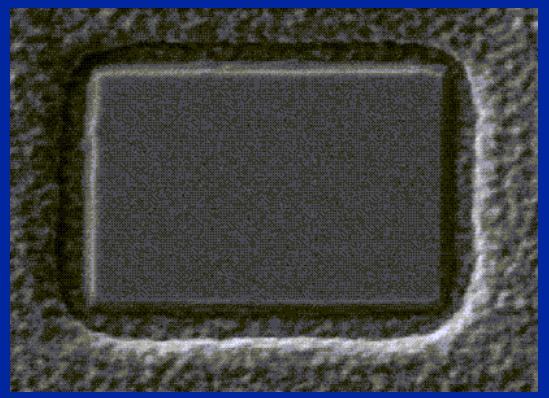


Increased wafer volume generated Ge deposits on chamber walls: Fixed with purges and pre-coats

OLD Process
After epi dep



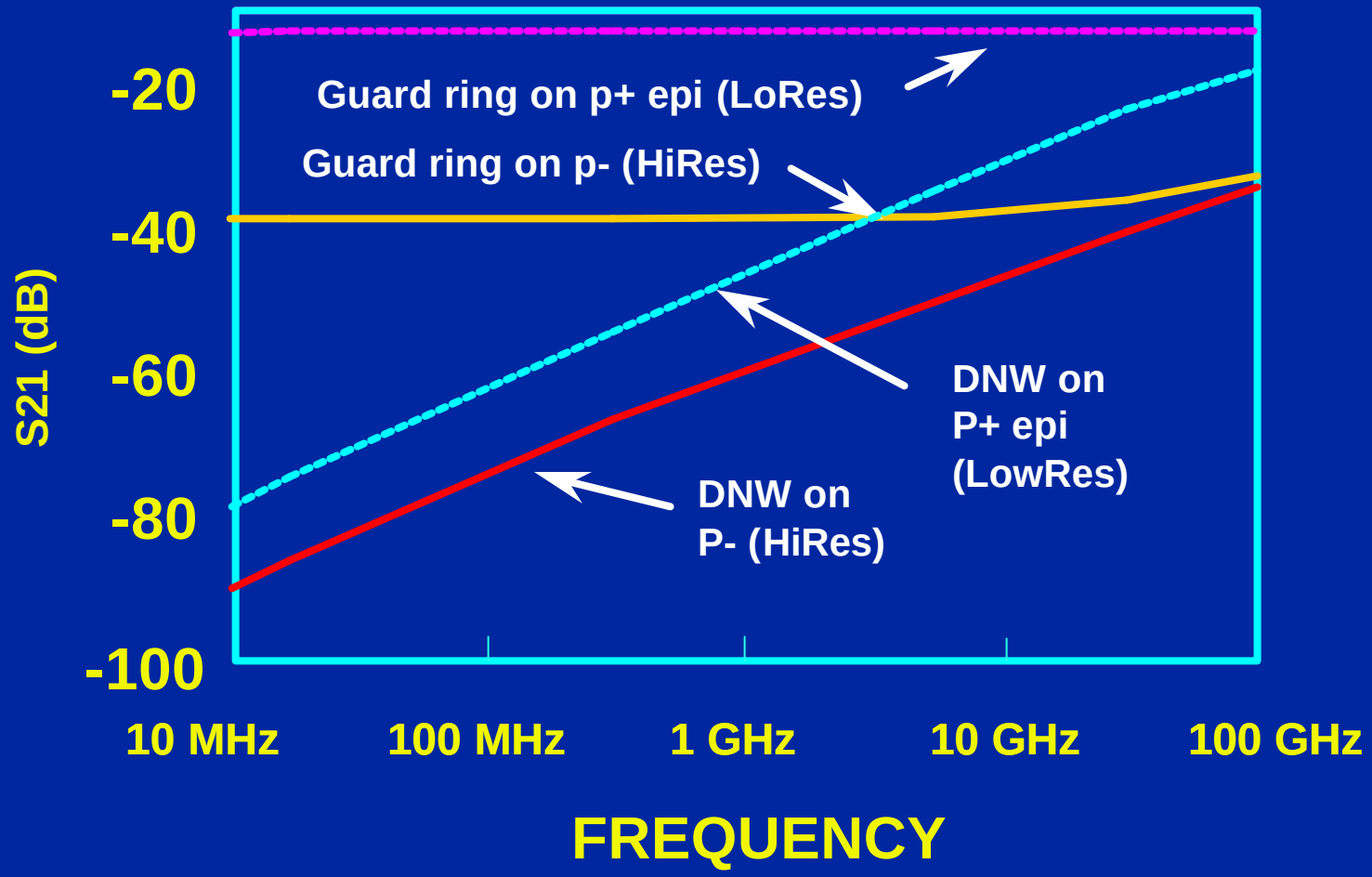
NEW Process
After epi dep



Outline

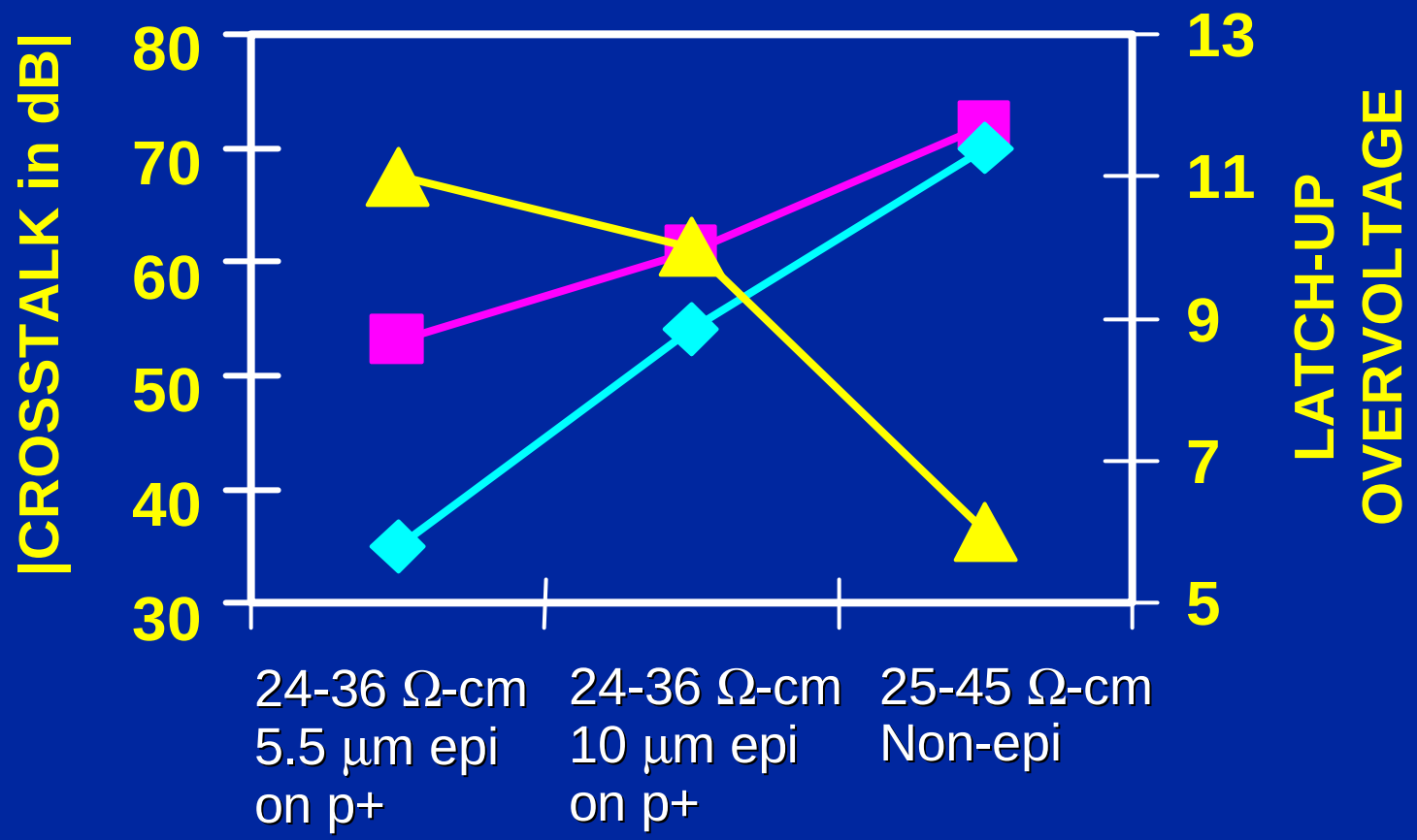
- Technology Features
- CMOS
- SiGe:C HBT
- Isolation

Isolation: P- versus P+ epi (with DNW)



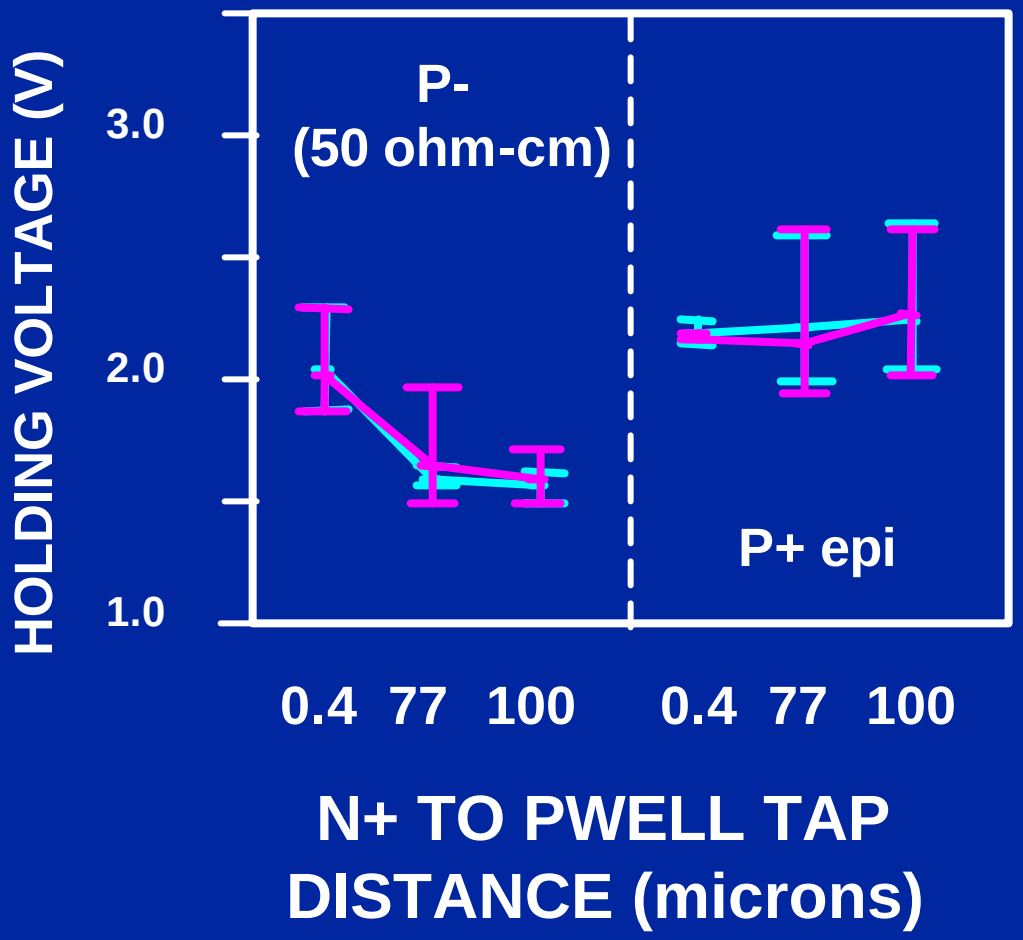
S21 = forward transmission gain/loss

Substrates: Latch-up, P- versus P+ epi



Merrill, R.B.; Young, W.M.; Brehmer, K. **Effect of substrate material on crosstalk in mixed analog/digital integrated circuits** Electron Devices Meeting, 1994.

Substrates: Latch-up, P- versus P+ epi with and without DNW

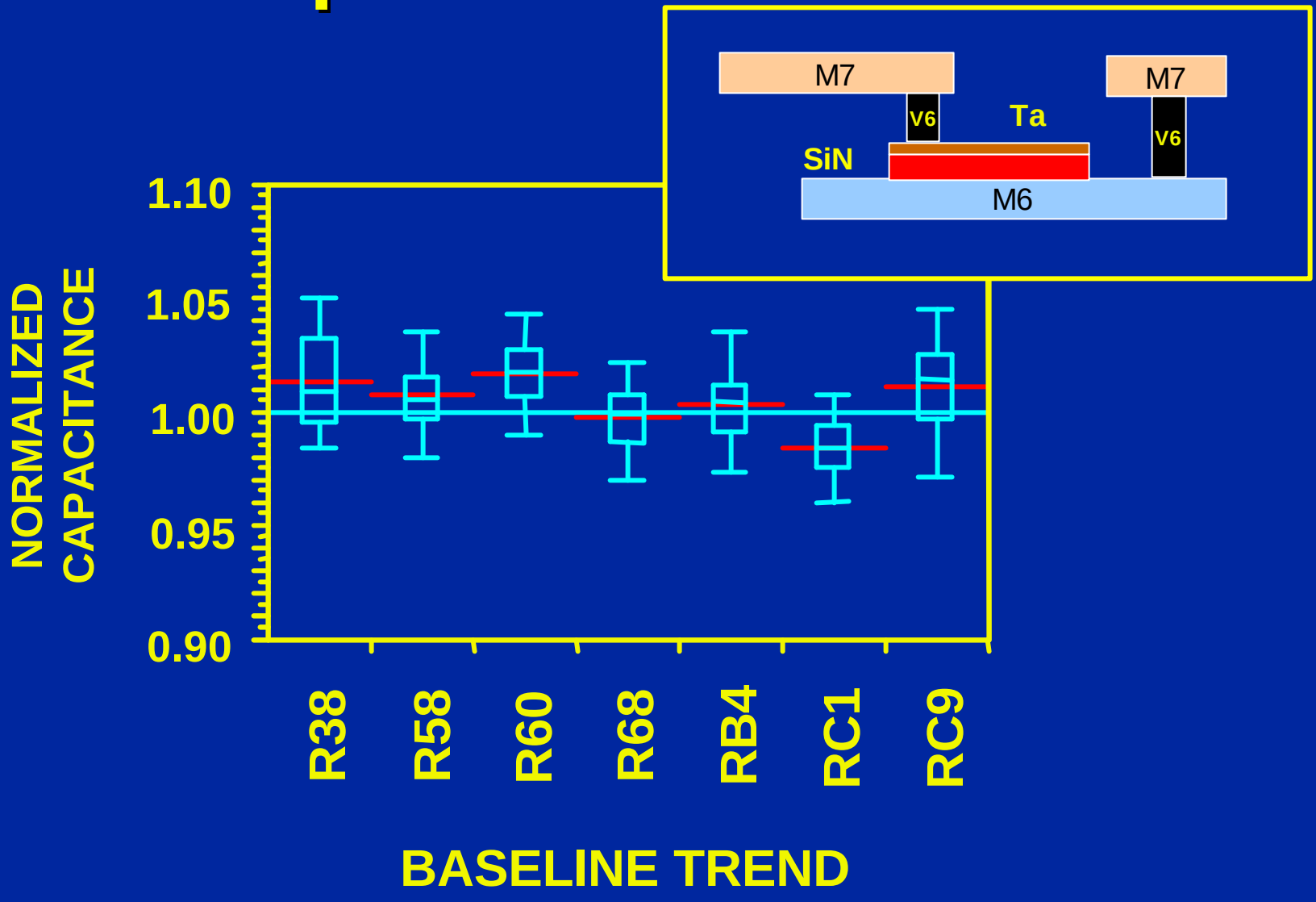


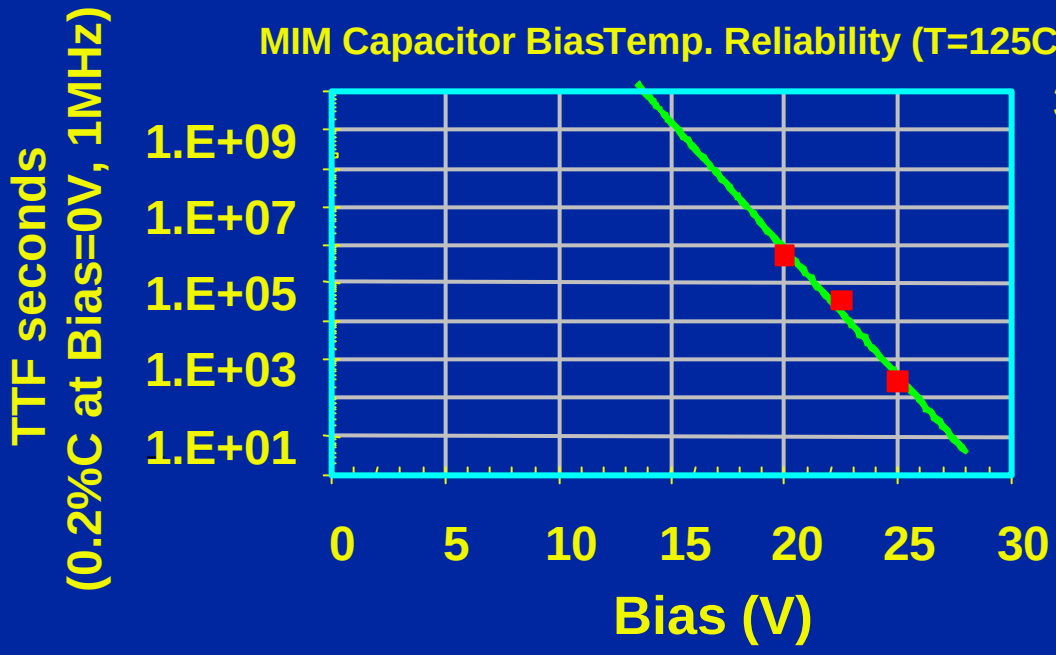
DNW (magenta)
No DNW (cyan)

Outline

- Technology Features
- CMOS
- SiGe:C HBT
- Isolation
- Passives

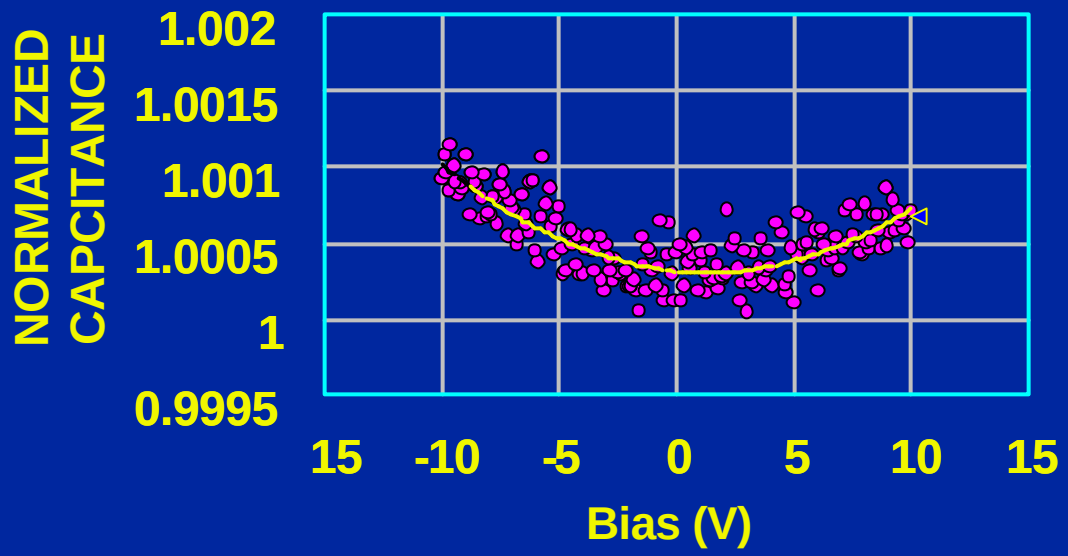
MIM Capacitor





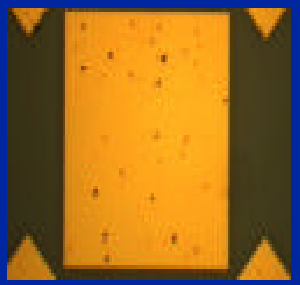
< MIM Cap Bias Temp.

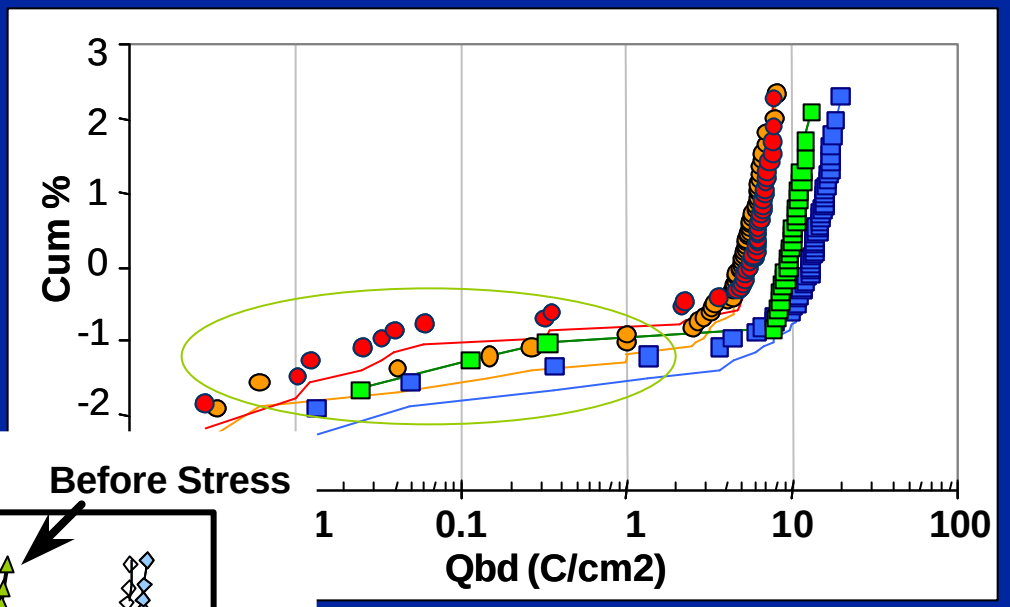
MIM Cap CV >

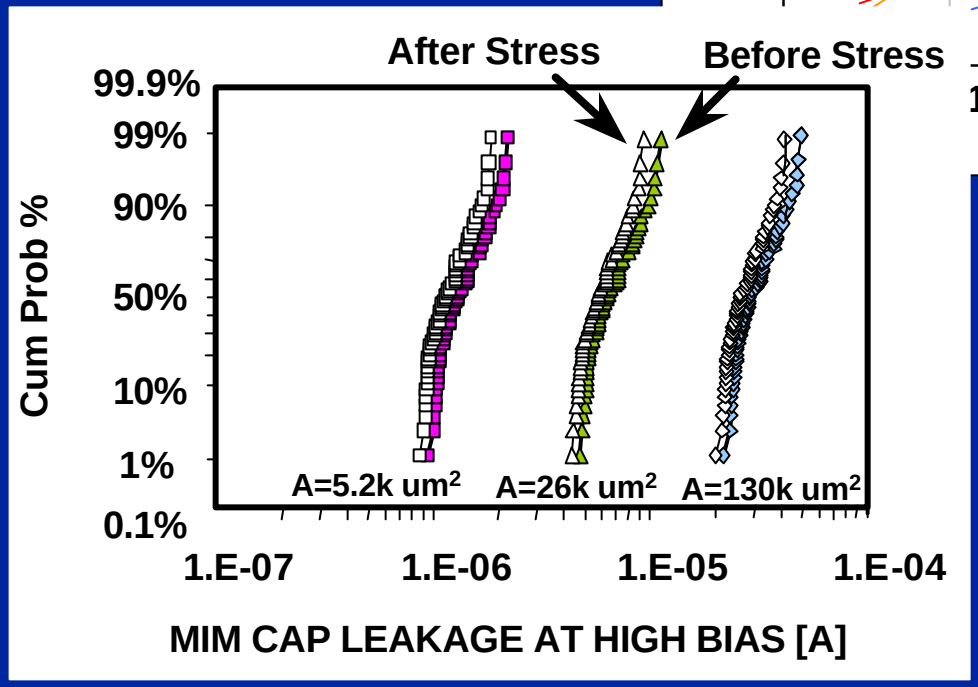


MIM Capacitor Reliability

OLD Process >

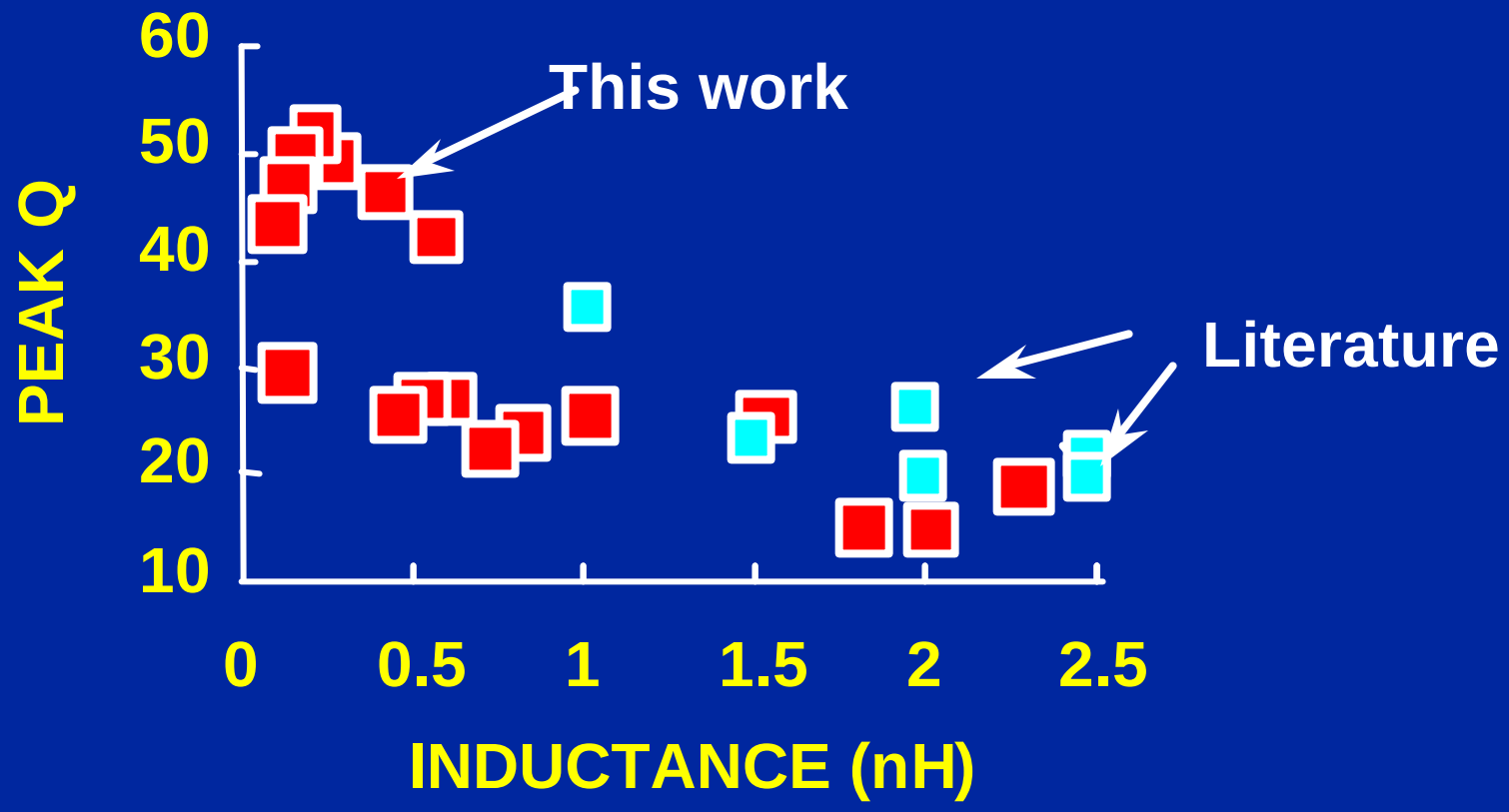






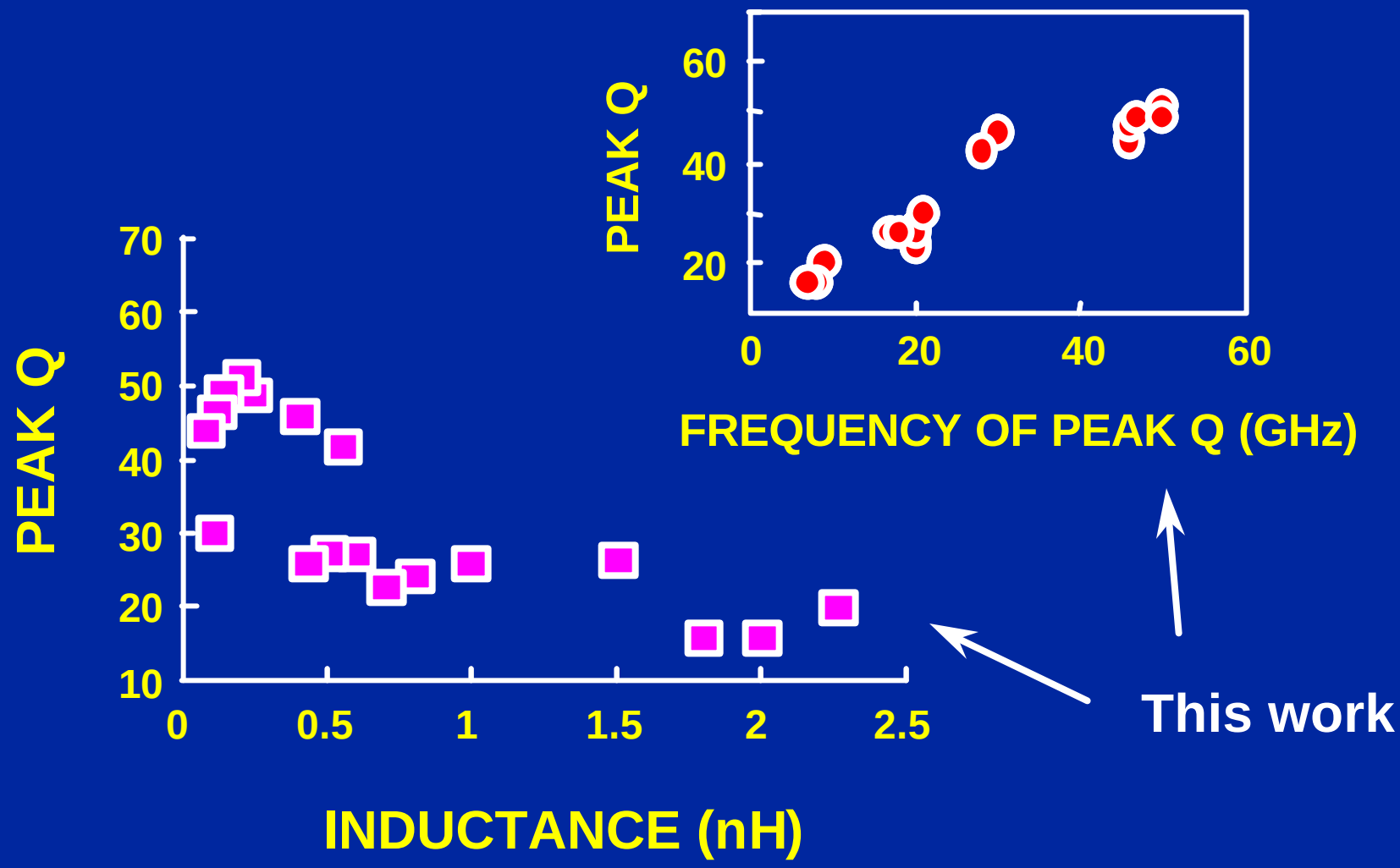
< New Process

Hi-Q Inductor Library Templates

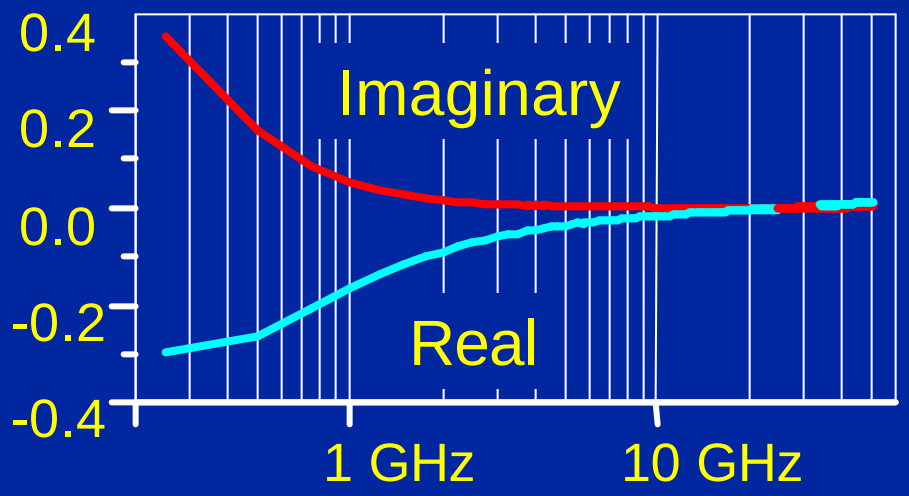


Focusing on lower L, Hi-Q inductors to support 10/40G circuits

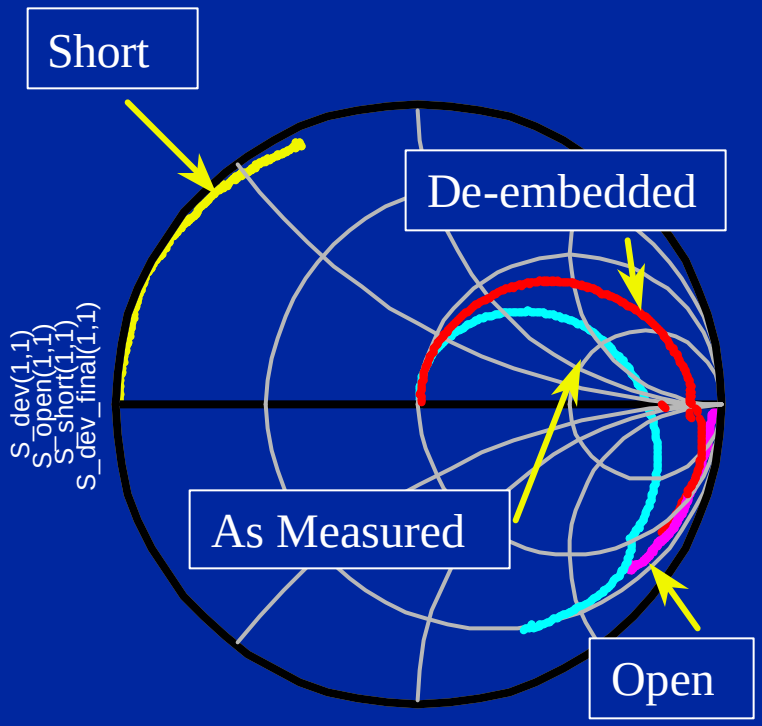
Hi-Q Inductor Library Templates



Measuring Q

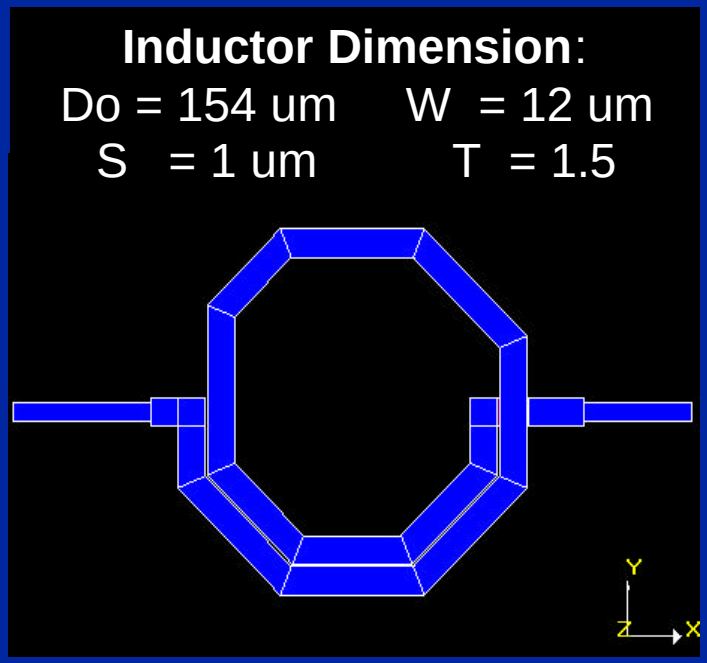


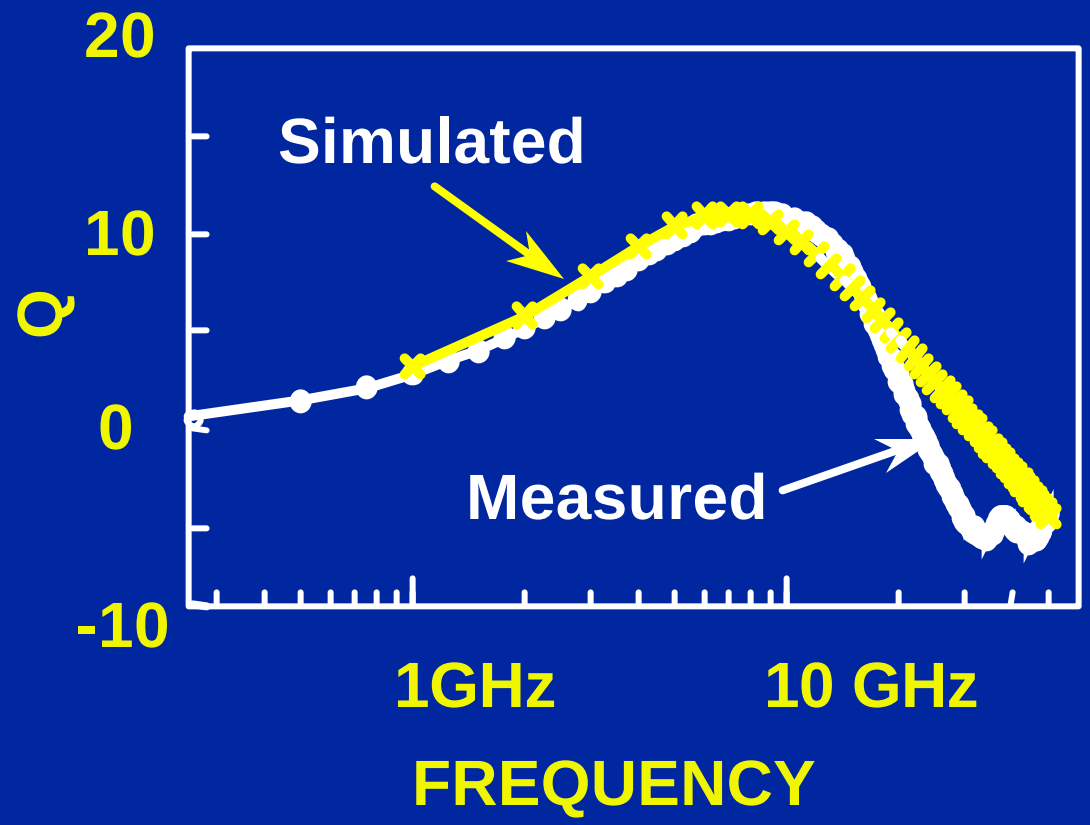
$$Q = \frac{-\,\mathrm{Im}\,(Y11)}{\mathrm{Re}\,(Y11)}$$



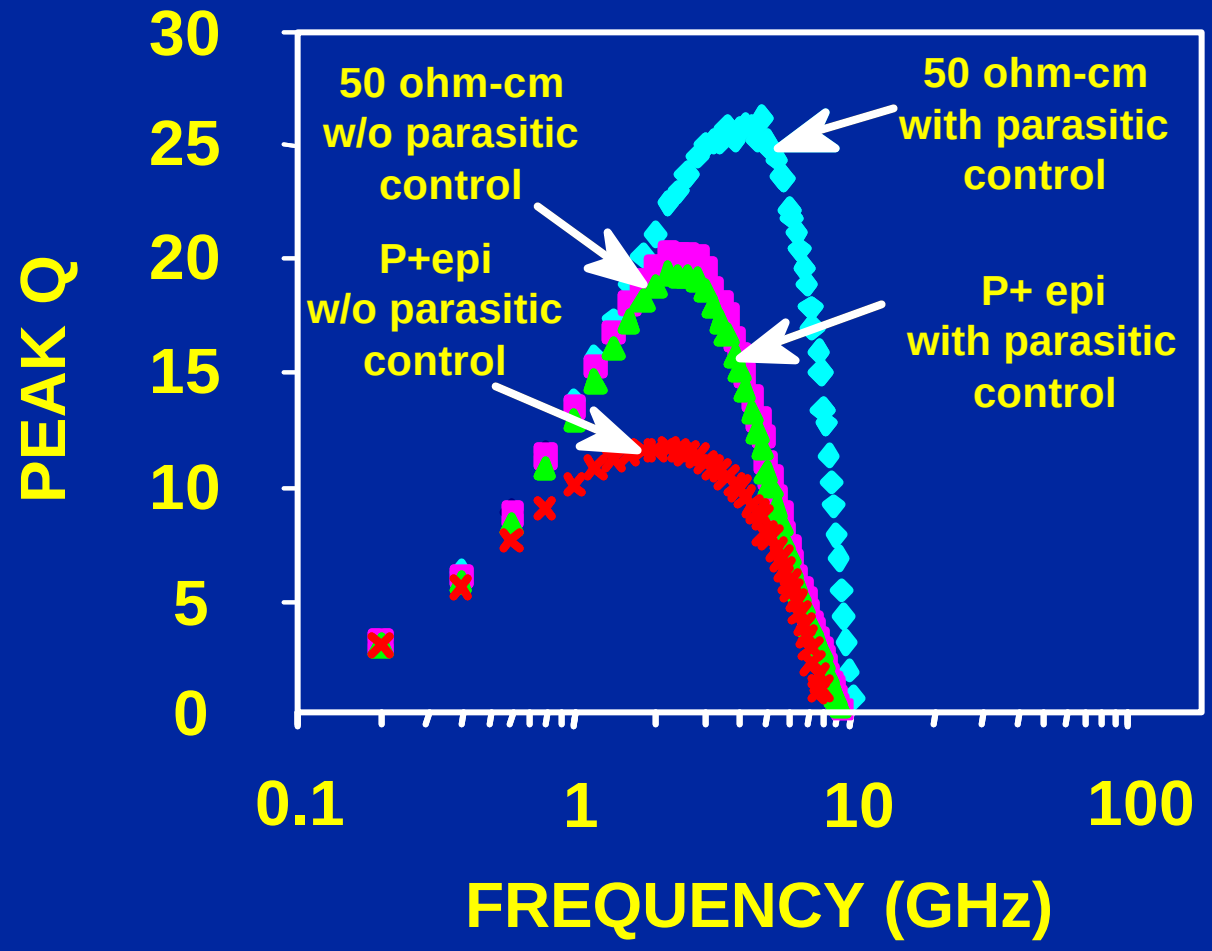
FREQUENCY
(250.0MHz to 50.25GHz)

Measured versus simulated Q





Hi-Q Inductors and substrates



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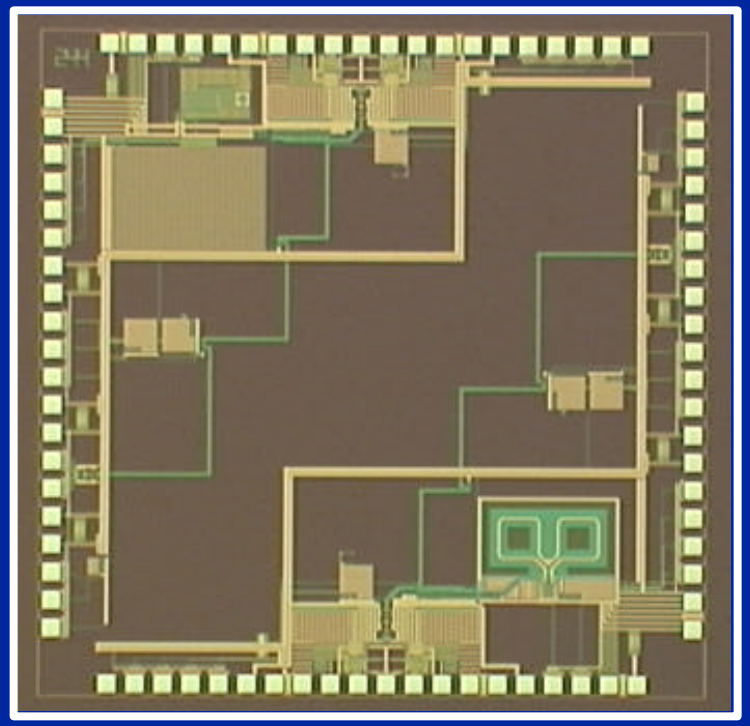
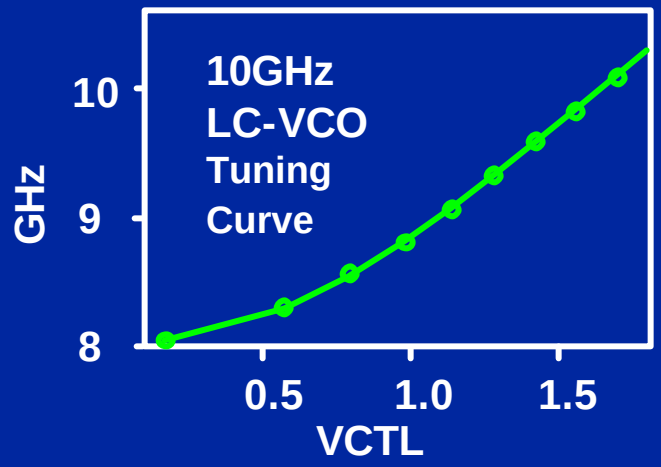
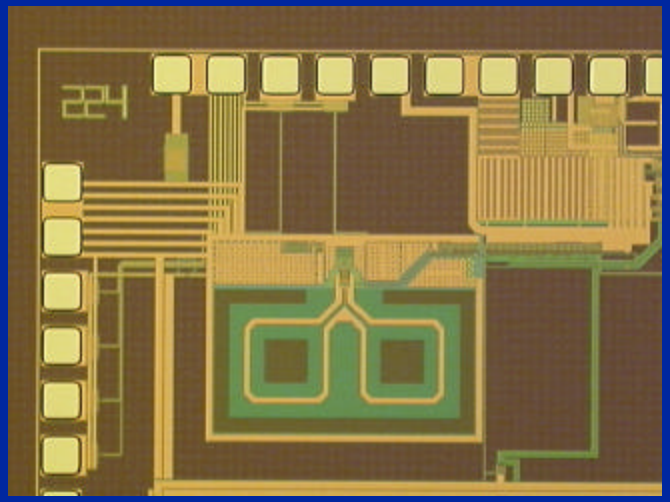
- Conclusions

Validation vehicles



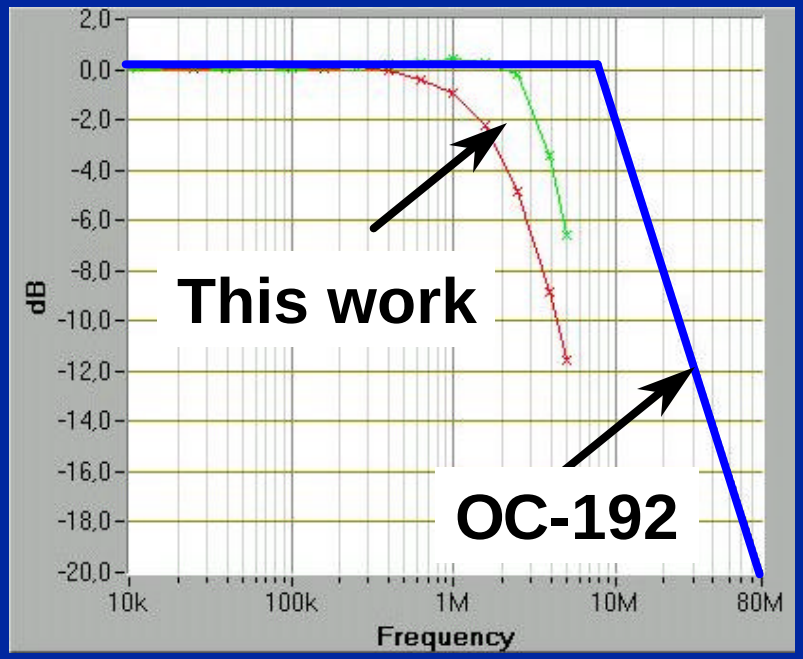


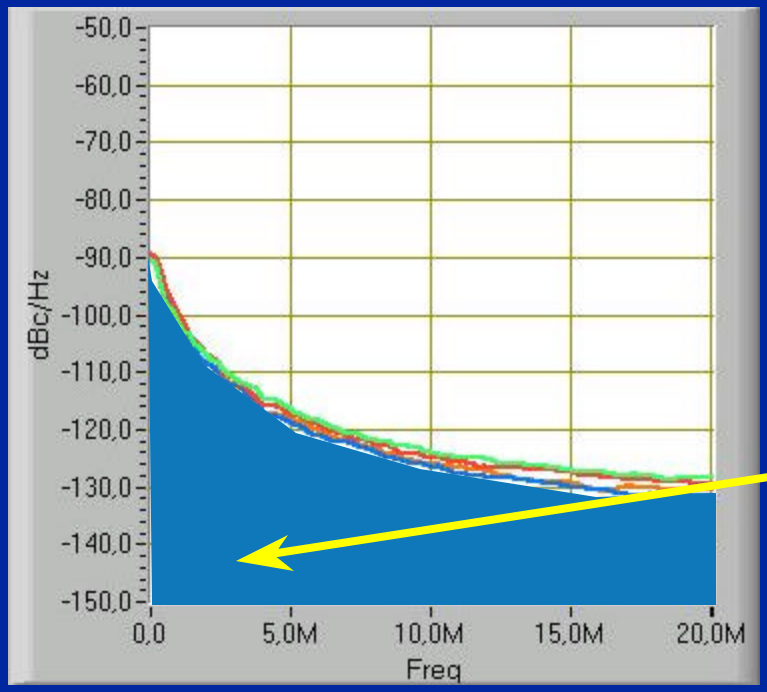


A large variety of learning vehicles are being supported
Illustrated is an LC-VCO from a 10G SerDes test circuit

Intel CMOS 10G SerDes Test Circuit Transmit PLL – Measured Jitter

Meets jitter transfer function specification >





OC-192 Specification is integral under curve = 100 mUI; Actual performance is 40 mUI ~ 2X better

Conclusions

- Manufacturable communications process integrated into 90nm digital CMOS
- RF NMOS devices at 225/140 F_T/F_{MAX}
- RF PMOS devices at 114/70 F_T/F_{MAX}
- Baseline HBT device at 130/100 F_T/F_{MAX}
- Reliable 1.15 fF/μm^2 Cu-MIM and resistor
- Hi-Q inductors

Acknowledgment

The authors gratefully acknowledge the many people at Intel who contributed to this work, including individuals from the following organizations:

- PTD Process and Design Groups
- Sort Test Technology Development
- Quality and Reliability Engineering
- Technology Computer Aided Design

References

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